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(54) Synchronization signal detector, synchronization signal detecting method and demodulator.

(57) A synchronization detector includes a NRZI circuit (2) for extracting edge portions of RF signals detected as binary-valued signals to form a pulse train, a counter (6) for counting the number of channel clocks in the distance between transitions represented by the edge portions, a latch circuit (5) operated responsive to pulses from the NRZI circuit for holding a number of previously counted channel clocks immediately preceding a current count of channel clocks, and AND gates (7, 8, 9, 10, 11, 12) and an OR gate (13) for detecting synchronization signals when the combination of the channel clocks from the counter and the latch circuit is the combination of the maximum distance between transitions Tmax and Tmax-kT (k = 1 or 2) of a (d, k ; m, n ; r) modulation code. Synchronization signals may be detected promptly even if the frame structure is increased in size to enable restoration of synchronization to be expedited when frame structure synchronization is not in order. A demodulator utilizing the synchronization signal detector is also disclosed.

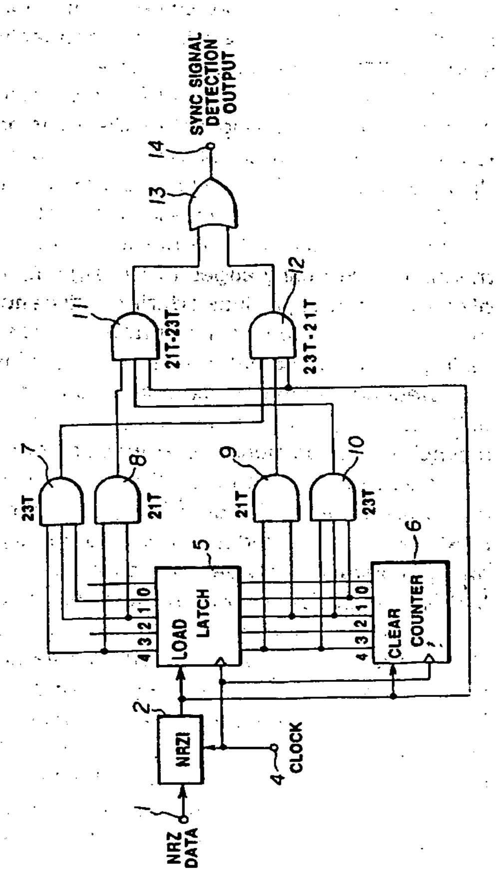

FIG.1

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This invention relates to a synchronization signal detector for detecting synchronization signals (such as frame synchronization signals), a method for detecting the synchronization signals, and a demodulator for demodulating data.

An eight-to-fourteen modulation (EFM) system is employed in a disc recording system for so-called compact discs (CD), or one of the other disc-shaped recording media, such as optical discs, magnetic discs or magneto-optical discs. With this modulation system, data are processed on the basis of units or strings of 8 bits, and each 8-bit bit string is translated into a string of 14-channel bits.

The recording format for a CD is shown in Fig. 12 and in Table 1, in which 24 channel bit synchronization signals (frame synchronization signals), 14 channel bit sub-coding data, 336 (24 x 14) channel bit data and 112 (8 x 14) channel bit parity data are furnished. In addition, 3 bits each are furnished as margin bits for connecting the pattern data, thus totalling 102 channel bits. One of the roles of the margin bits is to adjust the maximum distance between transitions of magnetization Tmax = 11 T in order not to be repeated twice for the synchronization signals. The encoding efficiency and the redundancy of this recording format are 57.1% and 42.9%, respectively.

TABLE 1

	data	channel bit
sync signals	-	24
subcoding	8	14
data	192	336
parity	64	112
margin bits	-	102
total	264	588

The above-mentioned CD recording format is disadvantageous in that: there is only one synchronization signal; margin bits are required for connecting the synchronization signals; and an exceptional bit string is set aside for the synchronization signals.

Meanwhile, each frame of the CD recording format is composed of 588 channel bits, as shown above. If it is assumed that moving picture data is to be recorded on a CD-sized disc, and the recording format is pursuant to the CD recording format and has a frame length longer than that provided in the CD recording format, the distance between the synchronization signals in the frame structure is increased, so that, if the frame structure synchronization is not in order, data restoration tends to be delayed.

In accordance with the present invention, there is provided a synchronization signal detector comprising means for extracting edges of RF signals detected as binary-valued signals, means for counting the number of channel clocks produced during a distance between adjacent transitions defined by extracted edges, means for holding the count of the channel clocks generated during a distance between the transitions directly preceding the distance between the transitions for which the number of pulses is currently counted, and means for detecting synchronization signals from outputs of the counting means and said holding means, using two patterns as synchronization signals, one of which is a frame synchronization signal and the other of which is a synchronization signal for at least error correction.

In accordance with the present invention, there is also provided a demodulating device for demodulating a variable length code comprising a synchronization signal detector section having means for extracting edges of RF signals detected as binary-valued signals, means for counting the number of channel clocks produced during a distance between adjacent transitions defined by extracted edges, means for holding the count of the channel clocks generated during a distance between the transitions directly preceding the distance between the transitions for which the number of pulses is currently counted, and means for detecting synchronization signals from outputs of the counting means and the holding means, using two patterns as synchronization signals, one of which is a frame synchronization signal and the other of which is a synchronization signal for at least error correction. The apparatus also comprises a timing controlling section for detecting the block boundary of said variable length code data based on detected synchronization signals, a data demodulating section for demodulating N-bit based variable length code data into M-bit based original data in accordance with a demodulation table performing an inverse conversion to the conversion prescribed by the modulation table used for encoding, based on the detected code length data and output data of the timing control section, and a match-

ing section supplied with the demodulated original data and an output of the timing control section as inputs for matching the original data to an external circuit.

Further respective aspects of the invention are set forth in the claims.

The invention will now be described by way of example with reference to the accompanying drawings, throughout which like parts are referred to by like references, and in which:

Fig. 1 is a schematic block circuit diagram showing a synchronization signal detector according to an embodiment of the present invention;

Fig. 2 illustrates a frame structure and the unit of an error correction coding;

Fig. 3 illustrates an entire recording format;

Fig. 4 illustrates an example of synchronization signals;

Fig. 5 illustrates another example of synchronization signals;

Fig. 6 illustrates conversion of NRZ data into NRZI data;

Fig. 7 illustrates conversion of the synchronization signals into NRZI data;

Fig. 8 illustrates the operation of a counter and a latch circuit of the synchronization signal detector;

Fig. 9 illustrates a synchronization pattern in NRZI representation;

Fig. 10 illustrates the operation of the counter and the latch circuit at the time of detection of synchronization signals;

Fig. 11 is a schematic block circuit diagram showing a decoder; and

Fig. 12 illustrates a CD recording format.

Referring to the drawings, preferred embodiments of the synchronization detector, method for detecting synchronization signals and the decoder relevant to the synchronization detector are explained in detail.

Referring to Fig. 1, the synchronization detector of the present embodiment includes a non-return-to-zero inverted (NRZI) circuit 2, as edge detection means, for extracting edges of detected binary-valued RF signals to generate a pulse train, a counter 6 for counting the number of channel clocks T of the distance between transitions which is the distance between the edges extracted from the NRZI circuit 2, that is the number of channel clocks T applied via terminal 4, a latch circuit 5 operated responsive to the pulses from the NRZI circuit 2 to hold the number of channel clocks corresponding to the distance between transitions directly preceding the distance between transitions being counted by counter 6, and AND gates 7 to 12 and an OR gate 13 for detecting synchronization signals from an output of the counter 6 and/or latch circuit 5 using two different patterns as synchronization signals for error correction, with one of the patterns being used as a frame synchronization signal and the other pattern as the synchronization signal for error correction.

The modulation coding employed in the present embodiment is a variable length coding (d, k; m, n; r) having different code word lengths depending on input data word lengths. Before proceeding to the description of the arrangement shown in Fig. 1, the variable length coding is explained.

The variable length coding is expressed as (d, k; m, n; r) in which d, k means a constraint imposed on a train of the same symbol information, d means the minimum length of a symbol "0", k means the maximum length of the symbol "0", m means the basic data length, n means the basic code length, n/m means a conversion ratio and r means the basic data length of conversion (constraint length). For example, the so-called 2-7RLL employed in a hard disc is expressed as (2, 7; 1, 2; 4) code.

In the present embodiment, (4, 22; 2, 5; 5) code is employed as the (d, k; m, n; r) code.

The data and the conversion table with the (4, 22; 2, 5; 5) code is shown in Table 2.

TABLE 2

	data	translation code
r=1	11	00000
	10	10000
	111111	000010000100000

r=2	0111	0100000000
	0110	0010000000
	0101	0001000000
	0100	0000100000
r=3	001111	010000100000000
	001110	010000010000000
	001101	010000001000000
	001100	010000000100000
	001011	000100000100000
	001010	001000010000000
	001001	001000001000000
	001000	001000000100000
	000111	000100001000000
r=4	00011011	01000010000100000000
	00011010	01000010000010000000
	00011001	01000010000001000000
	00011000	01000010000000100000
	00010111	01000000100000100000
	00010110	01000001000010000000
	00010101	01000001000001000000
	00010100	01000001000000100000
	00010011	01000000100001000000
	00010010	00100001000010000000
	00010001	00100001000001000000
	00010000	00100001000000100000
	00001111	00010000010000100000
	00001110	00100000010000100000
	00001101	00100000100001000000
	00001100	00100000100000100000
	00001011	01000000010000100000
	00001010	00001000010000100000
	00001001	00010000100001000000
	00001000	00010000100000100000
r=5	0000011111	0100001000010000100000000
	0000011110	0100001000010000010000000
	0000011101	0100001000010000001000000
	0000011100	0100001000010000000100000
	0000011011	0100001000000100000100000
	0000011010	0100001000001000010000000
	0000011001	0100001000001000001000000
	0000011000	0100001000001000000100000
	0000010111	0100001000000100001000000
	0000010110	0100000100001000010000000
	0000010101	0100000100001000001000000
	0000010100	0100000100001000000100000
	0000010011	0100000010000010000100000
	0000010010	0100000100000010000100000
	0000010001	0100000100000100001000000
	0000010000	0100000100000100000100000

0000001111	01000010000000010000100000
0000001110	0100000001000010000100000
0000001101	01000000010000100001000000
0000001100	01000000010000100000100000
0000001011	00100001000000100001000000
0000001010	00100001000010000010000000
0000001001	00100001000010000001000000
0000001000	00100001000010000000100000
0000000111	00100001000000100000100000
0000000110	00100001000000010000100000
0000000101	00100000010000100001000000
0000000100	00100000010000100000100000
0000000011	00100000001000010000100000
0000000010	00010000100000010000100000
0000000001	0001000010000100001000000
0000000000	00010000100001000000100000
	00010000001000010000100000
	0000100001000010000100000

In the present embodiment described herein, a recording format having a frame structure which becomes larger than the frame of the above-described EFM recording format for CD is taken as an example. The recording format of the present embodiment employs a block consisting of two frames as a unit for error correction codes, as shown in Fig. 2. Table 4 shows an arrangement of a sector (= 26 frames) and Fig. 3 shows an overall format.

TABLE 3

	data	channel bit
sync signals	-	100
sector mark/sector address	256	640
data	1024	2560
parity	256	640
DC control	-	120

TABLE 4

	data	channel bit
sync signals	-	1300
sector mark/sector address	256	640
data	16384	40960
parity	3328	8320
DC control	-	1560
total	19968	52780

Referring to Table 3 and Fig. 2, the recording format of the present embodiment includes, in the first two frames, 100 channel bit synchronization signals, 640 channel bit sector mark addresses, 2560 channel bit data and 640 channel bit parity data. Also, there are furnished a sum total of 120 channel bits between the patterns as DC control data. Each sector includes 1300 channel bit synchronization signals, 640 channel bit sector mark sector addresses, 40960 channel bit data, 8320 channel bit parity data and 160 channel bit DC control data. The coding efficiency and redundancy of the present format are 7.6% and 22.4%, respectively.

According to Table 2, it can be seen that consecutive data strings translate to channel bits. These channel bits, under this code, are sets of contiguous "0" channel bits separated by a single "1" channel bit, where each "1" channel bit represents a transition of magnetization. By placing various data strings together, it can be seen that there is a maximum distance between transitions of magnetization (Tmax) and a minimum distance between transitions of magnetization (Tmin). Under modulation by the above-mentioned (4, 22; 2, 5; 5) code, Tmax = 32 and Tmin = 5.

For the synchronization signal (frame synchronization pattern) to use in the case of modulation by the above-mentioned (d, k; m, n; r) code, it is necessary to select a pattern in which the maximum distance between transitions of magnetization Tmax is not increased, and the minimum distance between transitions of magnetization Tmin is not excessively decreased. Also, the pattern should not appear in the modulated data and preferably the pattern has a minimum length.

With the present embodiment, possible examples of long bit lengths (lengths of contiguous "0" bits) appearing in data, with the modulation by above-mentioned (d, k; m, n; r) code as the frame synchronization pattern, are those shown in Figs.4 and 5.

The examples of Fig. 4 and Fig. 5 of long bit continuation with the modulation by the (4, 22; 2, 5: 5) are the stream of channel bits of ...

"0100000000000000000001000000000000000000000001000000000
0000000000000100000"

for the data strings of ... 0111", "11", "11", "0111", "11", "11", "0100", "11", "11", "0100", ..., as shown in Fig. 4, and the channel bits of ...

"01000000000000000000001000000000000000000
0001000000"

for the data strings of ... "0111", "11", "11", "0111", "11", "11", "0101", "11", "11", "0100", ..., as shown in Fig. 5.

It is seen from Fig. 4 that, should there appear 23 T, that is 22 contiguous "0" channel bits, the bit lengths before and after it are both 20T, which represents the maximum value, 19, of contiguous "0" channel bits that can appear before or after a 23T. It is also seen from Fig. 5 that, should there appear 22 T, that is 21 contiguous "0" channel bits, the bit lengths before and after it cannot exceed 21T, which represents up to a maximum value of 20 contiguous "0" channel bits.

It is seen from this that, among contiguous pattern strings each having a bit length not exceeding 23 T, where T denotes the distance between bits (channel clocks), that is a bit length not exceeding the maximum distance between transitions of magnetization Tmax = 23T, there are certain combinations of contiguous pattern strings which do not appear in the modulation by the above-mentioned (4, 22; 2, 5; 5) code.

Concrete examples of these combinations include a first combination of 22T and 22T (22T - 22T), a second combination of 23T and 21T or 21T and 23T (23T - 21T or 21T - 23T), a third combination of 23T and 22T or 22T and 23T (23T - 22T or 22T - 23T) and a fourth combination of 23t and 23T (23T - 23T).

If the number of bits is increased, pattern string combinations other than the first to fourth combinations may also be contemplated, such as 22T - 21T - 21T combination. However, this leads to increased redundancy. For this reason, the data string combinations with the least possible number of bits are employed in the present embodiment.

It is mandatory, in this embodiment, that patterns which never appear in data be used as the frame synchronization signals (synchronization signals). With the present embodiment, this is taken into account when selecting the patterns of the frame synchronization signals among the above-mentioned first combination through fourth combination.

The frame synchronization patterns employed in the present embodiment are characterized in that the patterns can be formed by a bit length ("0" continuation) which is less than the maximum distance between transitions of magnetization Tmax (first combination of 22T - 22T), in that they can be formed by a combination of

different bit lengths inclusive of a bit length equal to the maximum distance between transitions of magnetization Tmax (the second combination of 23T and 21T or 21T and 23T or the third combination of 23T and 22T or 22T and 23T) and in that they can be formed by a combination of two contiguous maximum distances between transitions of magnetization Tmax (fourth combination of 23T and 23T).

Since the present embodiment has no margin bit, such as that provided in the aforementioned CD format, the maximum distance between transitions of magnetization Tmax = 23T and the minimum distance between transitions of magnetization Tmin = 5T need to be satisfied solely by synchronization signals. Also, since the (4, 22; 2, 5: 5) code is a variable length type recording code based on the 2/5 modulation, it is desirable from hardware configuration considerations that the bit length be equal to multiples of 5.

From the foregoing consideration, the following two synchronization signals have been selected for the present embodiment.

That is, the combination of 23T, 21T and 6T is used as the synchronization signal A, while the combination of 21T, 23T and 6T is used as the synchronization signal B. The 6T of the synchronization signals A and B are the bits appended for tail adjustment for providing a bit length equal to multiples of 5.

As described above, with the recording format of the present embodiment, the frame length is longer than that with the above-mentioned CD recording format. For this reason, the parity data for error correction code is increased in volume and in need of 32 bytes in terms of data bits.

Consequently, if, with the recording format of the present embodiment, failure in synchronization is incurred due to readout errors, data demodulation cannot be achieved until detection of the next synchronization signals. With a larger frame length, the volume of lost data is also increased. For this reason, a frame is desirably of a shorter length.

In this consideration, the synchronization signals A and B are employed in the present embodiment in such a manner that the unit of parity appended for error correction coding (data and sector mark 16 x 10 bytes plus 32 parity bytes) may be in the form of 2 frames (with each frame being 16 x 5 bytes + 16 bytes). That is, the synchronization signal A is used for frame synchronization and synchronization of ECC parity data, while the synchronization signal B is used exclusively for frame synchronization.

By using plural synchronization signals, it becomes possible for the respective synchronization signals to take charge of different functions. In this manner, the frame synchronization signal may be set so as to be arbitrarily shorter than the length of a block to which error correction code data is appended, as a result of which the error correction code data construction may be increased in the number of the degrees of freedom without being limited by the frame length.

The synchronization signal detector of the present embodiment is a synchronization signal detector capable of detecting the above-mentioned synchronization signals A and B.

Returning to Fig. 1, showing the synchronization signal detector of the present embodiment, binary-valued signals, which are RF signals, produced by an optical pickup or a magnetic head reading signal recording regions or pits recorded on a recording medium, such as an optical disc, magnetic disc or a magneto-optical disc, in accordance with the above-depicted recording format of the present embodiment, and clipped at a constant level as a threshold level, are transmitted to an input terminal 1.

These binary-valued RF signals are supplied to the NRZI circuit 2 which is operated based on channel clocks from terminal 4 for producing a pulse train based on extracted edge portions of the binary-valued signals. If the binary-valued RF signals are taken as so-called non-return-to-zero (NRZ) signals, having their state inverted at the boundary of the bit information, a pulse train formed by extracted edge portions may be produced by the NRZI circuit 2 inverting the signal state only when the bit information has a value of "1", as shown in Fig. 6.

In other words, if the data supplied to the input terminal 1 is the NRZ data, where "1" and "0" stands for "H" and "L", respectively the data is converted into NRZI data by the NRZI circuit 2, where "1" means inversion and "0" means non-inversion. For example, if the NRZ data is a data string consisting of 5T, 23T and 17T, as shown in Fig. 7, the NRZ data is converted into NRZI data in such a manner that data "1" is present at the point of transition from "0" to "1" or from "1" to "0". In the example of Fig. 7, by conversion of the NRZ data into NRZI data, four "0"s are arrayed during 5T, 22 "0"s are arrayed during 23T and 16 "0"s are arrayed during 17T. Consequently, the aforementioned synchronization signal pattern has 22 "0"s followed by one "1" followed in turn by 20 "0"s, as shown in Fig. 9, or alternatively, 20 "0"s followed by one "1" followed in turn by 22 "0"s.

The pulse train from the NRZI circuit 2 is supplied to a clear terminal of the counter 6 and to a load terminal of a latch circuit 5. The channel clocks from terminal 4 are supplied to clock terminals of the counter 6 and the latch circuit 5.

The counter 6 has a count capacity of counting the number of the longest channel clocks of the transition patterns of the synchronization signals to be detected, and counts the number of the channel clocks T between the edges, that is the number of channel clocks between the edges (transition distances) extracted by the NRZI

circuit 2.

The latch circuit 5 holds the count value of the counter 6 (number of channel clocks) and transmits the value of the channel clocks (count value) held thereby to the next stage each time transition of the binary-valued RF signals is incurred, that is each time an edge extracted by the NRZI circuit 2 is encountered. In other words, the latch circuit 5 holds the value of the number of channel clocks (count value) corresponding to the distance between transitions directly preceding the distance between transitions being counted by the counter 6 and transmits the thus held count value to the next stage.

That is, since "1" stands for a point of run interruption, counter 6 counts up by +1 each time "0" data is encountered, while latch circuit 5 holds the count value from the counter 6. Conversely, if the data is "1", counter 6 is cleared, while the latch circuit 5 loads the count value from counter 5, that is the current count value.

The counter 6 and the latch circuit 5 are arranged in a 5-bit output configuration. That is, the output terminals of the counter 6 and the latch circuit 5 are connected to respective input terminals of AND gates 7 to 10.

Specifically, the output terminals of the counter 6 associated with first, second and fourth of the 0th to fourth bits of the five-bit output of the counter 6 are connected to the three input terminals of the AND gate 10, while the output terminals of the counter associated with the second and fourth bits are connected to the two input terminals of the AND gate 9. Also, the output terminals of the latch circuit 5 associated with first, second and fourth of the 0th to fourth bits of the five-bit output of the latch circuit 5 are connected to three input terminals of the AND gate 7, while the output terminals of the latch circuit 5 associated with the second and fourth bits are connected to the two input terminals of the AND gate 8.

The outputs of the AND gates 8 and 10 are supplied to two input terminals of a three-input AND gate 11, while the outputs of the AND gates 7 and 9 are supplied to two input terminals of a three-input AND gate 12. Outputs of the NRZI circuit 2 are supplied to the remaining input terminals of the AND gates 11 and 12. The NRZI data from the NRZI circuit 2 are used as timing signals in the AND gates 11 and 12.

With the present embodiment, the AND gates 7 to 10 detect 21T or 23T. On the other hand, the AND gates 11, 12 detect the synchronization signal when the combination of 21T and 23T or the combination of 23T and 21T is encountered and "1" is entered from NRZI circuit 2.

Outputs of the AND gates 11, 12 are transmitted to associated input terminals of the two-input OR gate 13. An ORed output of the OR gate 13 is output at output terminal 14 as a synchronization signal detection output of the present detector.

Specifically, the synchronization pattern consisting of the combination of 23T and 21T in the NRZI representation is detected as shown in Fig. 9.

Referring to Fig. 10, the NRZI data becomes "1" at a timing ta so that counter 6 is cleared to "0". The latch circuit 5 holds the directly previous count value by fetching the previous count value "22". At a timing tb, the synchronization signal is detected. That is, the count value becomes 20, while the latch circuit 5 holds the count value of "22" at a timing directly preceding timing tb. This count value, thus held by latch circuit 5, becomes the synchronization signal. If "1" appears in data at the timing tb, the synchronization signal is detected by the AND gates 7 to 12 and the OR gate 13.

It is seen from above that a 1-clock synchronization signal detection output is issued when the above data corresponding to the synchronization signal is entered. For example, when the synchronization pattern is a 23T - 21T combination, data is NRZI representation including 22 contiguous "0"s and 20 contiguous "0"s is detected. Similarly, when the synchronization pattern is a 21T - 23T combination, data in NRZI representation including 20 contiguous "0"s and 22 contiguous "0"s is detected.

The demodulating device of the present embodiment is now explained.

The demodulating device is a decoding device for decoding the above-mentioned variable length coded data and includes, as shown in Fig. 11, a synchronization signal detection circuit 22, arranged as shown in Fig. 1, a timing supervising circuit 23 for detecting the boundary between the blocks of the variable length coded data, based on the synchronization signals detected by the synchronization signal detector 22, and a code length detection circuit 24 for detecting the code length of the variable length coded data. The demodulating device also includes a data demodulating circuit 25 for demodulating the N-bit based variable length coded data into M-bit based original data in accordance with a demodulating table as a counterpart of the modulating table employed for variable length encoding based on the code length data detected by the code length detection circuit 24 and output data of the timing supervising circuit 23. Finally, the demodulating device includes an external interface 26 to which the original data demodulated by the data demodulating circuit 25 and an output of the timing supervising circuit 23 are entered and which effectuates matching between the original data and the downstream side circuit.

Referring to Fig. 11, data read out from a recording medium, such as an optical disc, are supplied to an input terminal 21. The above-mentioned synchronization signals are detected by the synchronization signal

detector 22 from data supplied thereto. Based on the synchronization signals, detected by detector 22, the timing control circuit 23 generates timing signals employed for timing control during data demodulation.

Since it is necessary with the variable length coding to detect code length for data demodulation, the code length is detected by the code length detection circuit 24.

Using the code length data from the code length detection circuit 24 and the timing signals from the timing control circuit 23, the data demodulating circuit 25 demodulates data supplied to input terminal 21. Demodulated data from data demodulating circuit 25 are transmitted to the external interface 26 which effectuates matching with the downstream side circuit based on the timing signals. By way of an example, the external circuit 26 translates the 10-bit data from the data demodulating circuit 25 into 8-bit data to output the resulting data. An output of the external interface 26 is output at output terminal 27 as demodulated data.

It is noted that the variable length codes of the present embodiment are employed in a format employed for recording moving picture data on e.g. a compact disc (CD).

Although the present invention has been shown and described with respect to preferred embodiments, various changes and modifications which are obvious to a person skilled in the art to which the invention pertains are deemed to lie within the scope of the invention as claimed.

Claims

1. A synchronization signal detector for detecting synchronization signals embedded in radio frequency (RF) signals containing data encoded according to a modulation table, the synchronization signal detector comprising:

   means (2) for extracting edges of the RF signals detected as binary-valued signals,

   counting means (6) for counting a number of channel clocks generated by an external channel clock generator between adjacent extracted edges,

   holding means (5) for holding a count of the channel clocks previously counted by the counting means while the counting means counts a current number of channel clocks generated between adjacent extracted edges, and

   means (7,8,9,10,11,12,13) for receiving outputs of the counting means (6) and the holding means (5) and for detecting synchronization signals by comparing the outputs of the counting means (6) and the holding means (5) with synchronization signals comprising two patterns, one pattern representing a frame synchronization signal and the other pattern representing a synchronization signal for at least error correction.

2. A synchronization signal detector as claimed in claim 1, wherein each of the two patterns comprises a combination of bit counts not present in the encoded data, bit lengths representing clocks counted between extracted edges in the synchronization signals, each bit count being less than or equal to Tmax, which is the maximum number of clocks between extracted edges in the coded data, and greater than or equal to Tmin, which is the minimum number of clocks between extracted edges in the coded data, inclusive, the patterns also satisfying at least one of the following conditions (i) to (iii):

   (i) the patterns are each a combination of bit lengths smaller than a maximum number of bit counts between transitions of magnetization of the conversion code;

   (ii) the patterns are each a combination of different bit counts inclusive of Tmax; and

   (iii) the patterns are each a combination of Tmax and another Tmax contiguous thereto.

3. A synchronization signal detector as claimed in claim 1, wherein a modulation code used for encoding the encoded data is a variable length code having different code word lengths depending on input data word lengths, the variable length code being in the format of (d, k; m, n; r), where d, k means a constraint imposed on a train of the same symbol information (d means a minimum length of a symbol "0", k means a maximum length of the symbol "0"), m means a basic data length, n means a basic code length, and r means a basic data length of conversion (constraint length), and d, k, m, n, r, Tmax and Tmin have the following values:

   d = 4;
   k = 22;
   m = 2;
   n = 5;
   r = 5;
   Tmax = 23T and

Tmin = 5T.

4. A synchronization signal detector as claimed in claim 3, wherein a spacing between transitions in each of the two patterns comprises one of the following: 22 bits followed by 22 bits, 23 bits followed by 21 bits, 21 bits followed by 23 bits, 23 bits followed by 22 bits, 22 bits followed by 23 bits, and 23 bits followed by 23 bits.

5. A synchronization signal detector as claimed in claim 1, wherein a margin bit for tail adjustment is appended to each pattern.

6. A synchronization signal detector as claimed in claim 5, wherein a total number of bits of the pattern of each of the synchronization signals, including the appended margin bit, is equal to a multiple of five.

7. A demodulating device for demodulating variable length code data comprising:
a synchronization signal detector (22) comprising means (2) for extracting edges of radio frequency (RF) signals detected as binary-valued signals;
counting means (6) for counting a number of channel clocks generated by an external source between adjacent extracted edges;
holding means (5) for holding a count of the channel clocks previously counted by the counting means while the counting means counts a current number of channel clocks between adjacent extracted edges;
detecting means (7,8, 9, 10, 11, 12, 13) for receiving outputs of the counting means (6) and the holding means (5) and detecting synchronization signals by comparing the outputs of the counting means (6) and the holding means (5) with synchronization signals comprising two patterns, one pattern representing a frame synchronization signal and the other pattern representing a synchronization signal for at least error correction;
timing controlling means (23) for detecting a block boundary of variable length code data based on synchronization signals detected by the detecting means and for outputting timing control information;
code length detection means (24) for detecting a code length of the variable length data;
data demodulating means (25) supplied with the detected code length of the variable length data for demodulating the variable length code data into original data in accordance with a demodulation table used to decode the variable length encoded data, based on a detected code length data outputted by the code length detection means and timing control information output by the timing controlling means; and
matching means (26) for receiving as inputs demodulated original data output by the data demodulating means and the timing control information output by the timing controlling means and using the inputs for matching the original data to an external circuit.

8. A method for detecting synchronization signals embedded in radio frequency (RF) signals containing data encoded according to a modulation table, the synchronization signal detecting method comprising the steps of:
extracting (2) edges of the RF signals detected as binary-valued signals,
counting (6) a number of channel clocks generated by an external channel clock generator between adjacent extracted edges,
holding (5) a count of the channel clocks previously counted while counting a current number of channel clocks generated between adjacent extracted edges, and
receiving (7, 8, 9, 10, 11, 12, 13) current counts and held counts and detecting synchronization signals by comparing the current counts and the held counts with synchronization signals comprising two patterns, one pattern representing a frame synchronization signal and the other pattern representing a synchronization signal for at least error correction.

9. A synchronization signal detecting method as claimed in claim 8, wherein each of the two patterns comprises a combination of bit counts not present in the encoded data, bit lengths representing clocks counted between extracted edges in the synchronization signals, each bit count being less than or equal to Tmax, which is the maximum number of clocks between extracted edges in the coded data, and greater than or equal to Tmin, which is the minimum number of clocks between extracted edges in the coded data, inclusive, the patterns also satisfying at least one of the following conditions (i) to (iii):
(i) the patterns are each a combination of bit lengths smaller than a maximum number of bit counts between transitions of magnetization of the conversion code;
(ii) the patterns are each a combination of different bit counts inclusive of Tmax; and

(iii) the patterns are each a combination of Tmax and another Tmax contiguous thereto.

10. A synchronization signal detecting method as claimed in claim 8 wherein a modulation code used for encoding the encoded data is a variable length code having different code word lengths depending on input data word lengths, the variable length code being in the format of (d, k; m, n; r), where d, k means a constraint imposed on a train of the same symbol information (d means a minimum length of a symbol "0", k means a maximum length of the symbol "0"), m means a basic data length, n means a basic code length, and r means a basic data length of conversion (constraint length), and d, k, m, n, r, Tmax and Tmin have the following values:

d = 4;
k = 22;
m = 2;
n = 5;
r = 5;
Tmax = 23T and
Tmin = 5T.

11. A synchronization signal detecting method as claimed in claim 10 wherein a spacing between transitions in each of the two patterns comprises one of the following: 22 bits followed by 22 bits, 23 bits followed by 21 bits, 21 bits followed by 23 bits, 23 bits followed by 22 bits, 22 bits followed by 23 bits, and 23 bits followed by 23 bits.

12. A synchronization signal detecting method as claimed in claim 8 wherein a margin bit for tail adjustment is appended to each pattern.

13. A synchronization signal detecting method as claimed in claim 12 wherein a total number of bits of the pattern of each of the synchronization signals, including the appended margin bit, is equal to a multiple of five.

14. A synchronization signal detector for detecting synchronization signals embedded in radio frequency (RF) signals containing data encoded according to a modulation table, the synchronization signal detector comprising:

means (2) for extracting edges of the RF signals detected as binary-valued signals,

counting means (6) for counting a number of channel clocks generated by an external channel clock generator between adjacent extracted edges,

holding means (5) for holding a count of the channel clocks previously counted by the counting means while the counting means counts a current number of channel clocks generated between adjacent extracted edges,

means (7, 8, 9, 10, 11, 12, 13) for receiving outputs of the counting means and the holding means and for detecting synchronization signals by comparing the outputs of the counting means and the holding means with synchronization signals comprising two patterns, one pattern representing a frame synchronization signal and the other pattern representing a synchronization signal for at least error correction,

wherein the spacing between transitions in each of the two patterns comprises one of the following: 22 bits followed by 22 bits, 23 bits followed by 21 bits, 21 bits followed by 23 bits, 23 bits followed by 22 bits, 22 bits followed by 23 bits, 23 bits followed by 23 bits, and

wherein a margin bit for tail adjustment is appended to each pattern.

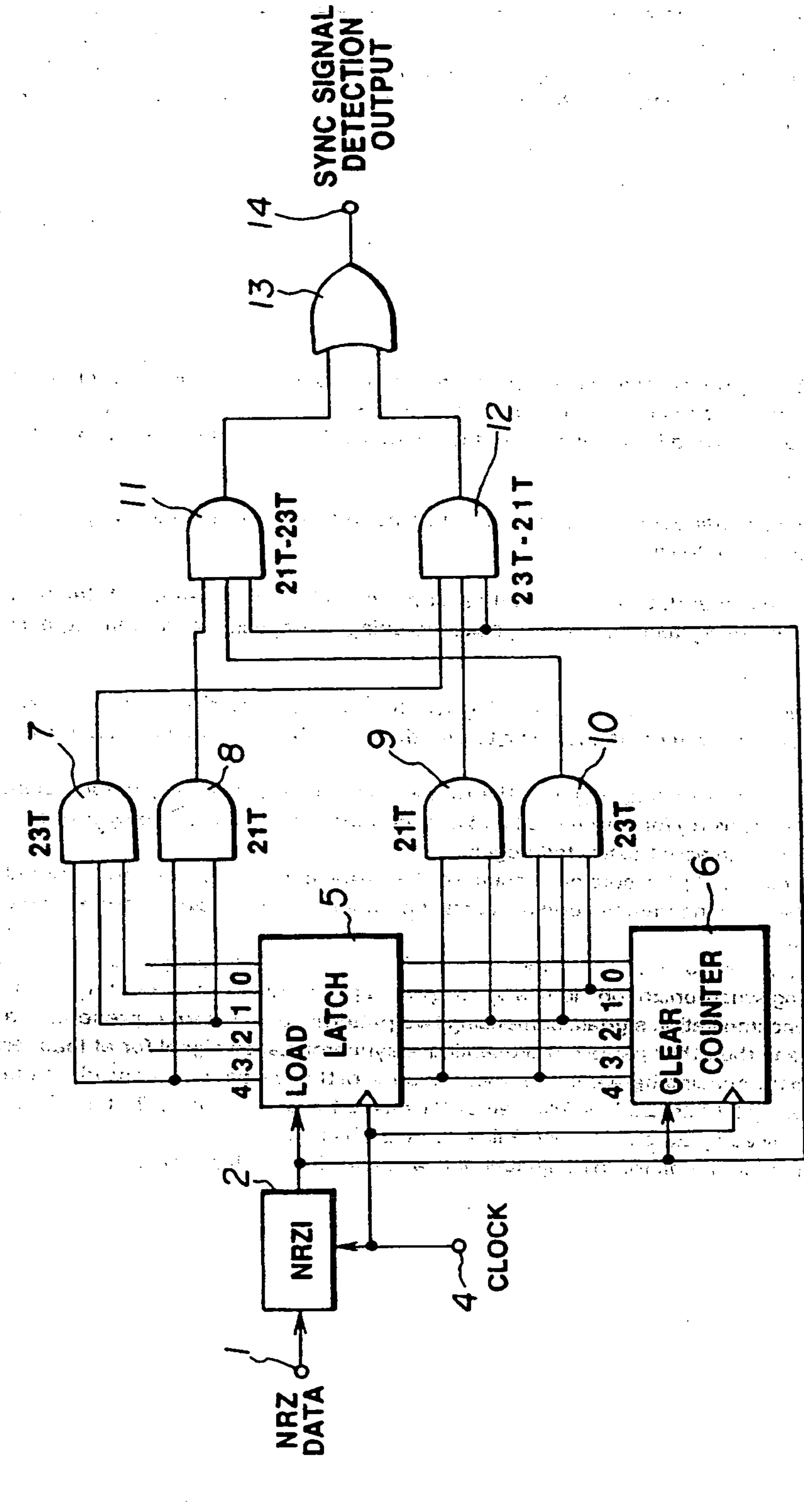
NRZ DATA
NRZI
CLOCK
LOAD
LATCH
CLEAR
COUNTER
23T
21T
21T
23T
21T-23T
23T-21T
SYNC SIGNAL DETECTION OUTPUT

FIG.1

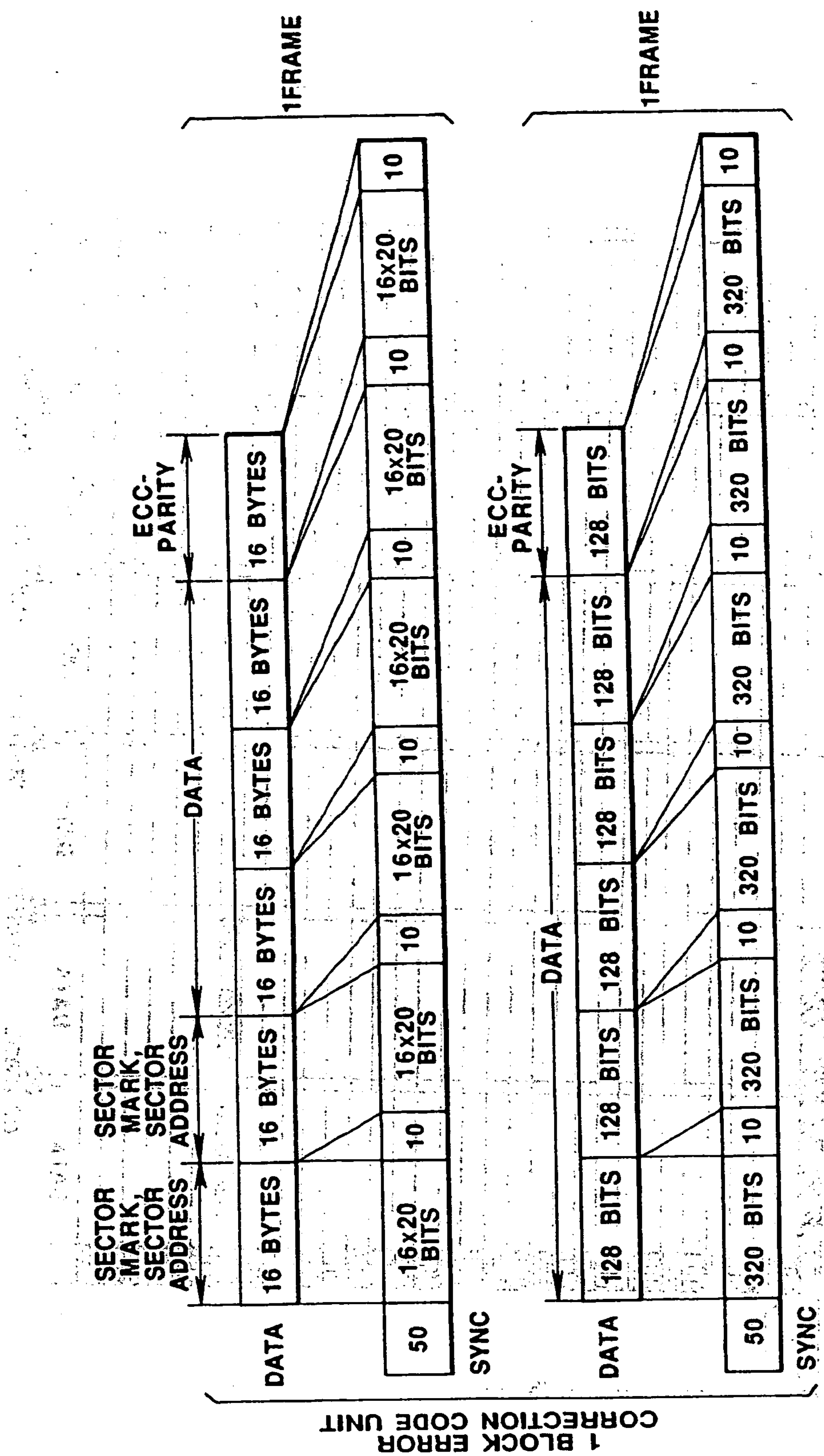
1FRAME
ECC-PARITY
DATA
SECTOR MARK, SECTOR ADDRESS
SECTOR MARK, SECTOR ADDRESS
DATA
16 BYTES
16 BYTES
16 BYTES
16 BYTES
16 BYTES
16 BYTES
SYNC
50
16x20 BITS
10
10
1FRAME
ECC-PARITY
DATA
128 BITS
128 BITS
128 BITS
128 BITS
128 BITS
128 BITS
SYNC
50
320 BITS
10
1 BLOCK ERROR CORRECTION CODE UNIT

FIG.2

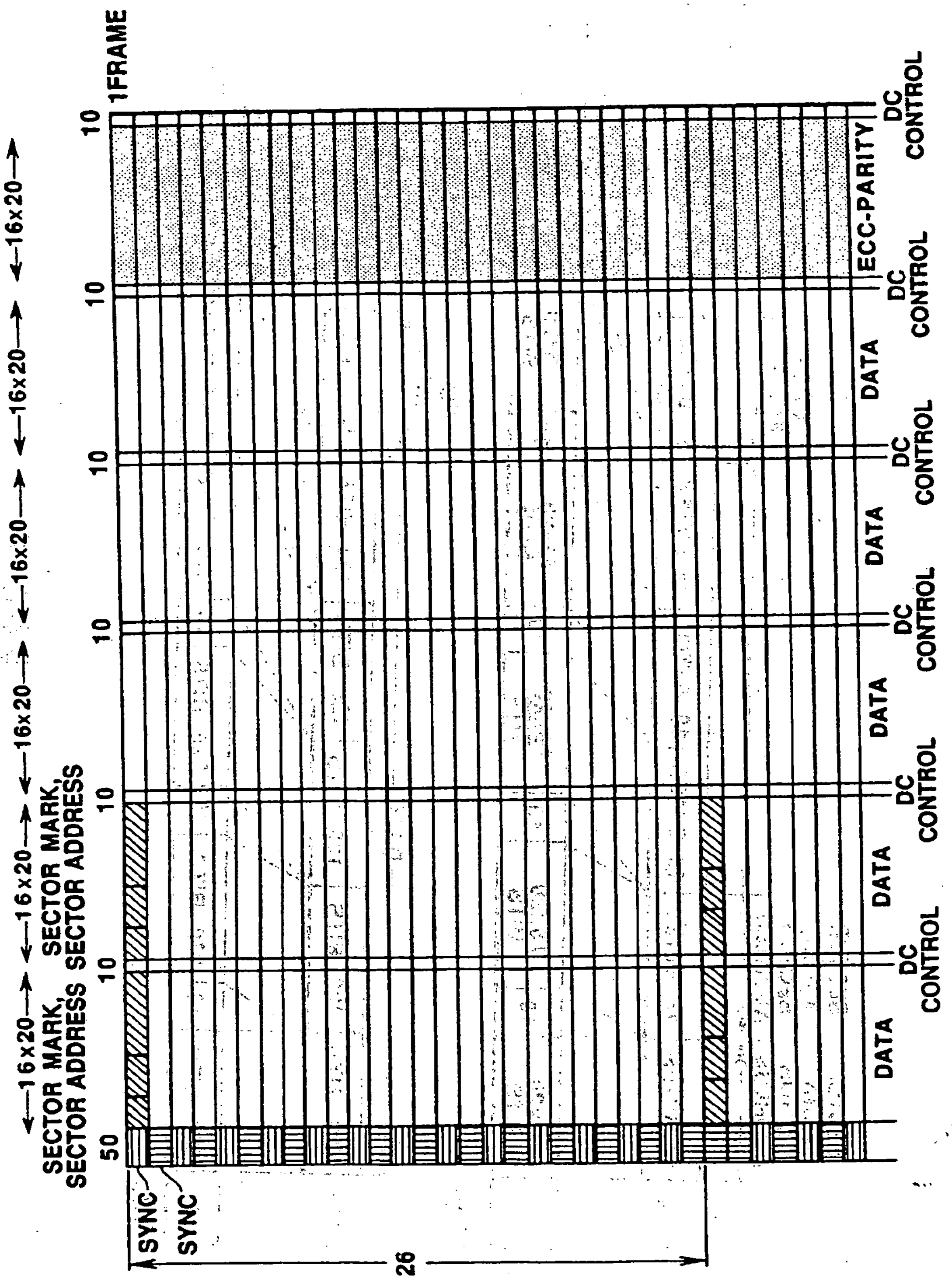
16x20
SECTOR MARK, SECTOR ADDRESS
16x20
SECTOR MARK, SECTOR ADDRESS
16x20
16x20
16x20
16x20
50
10
10
10
10
10
10
1FRAME
SYNC
SYNC
26
DATA
DC CONTROL
DATA
DC CONTROL
DATA
DC CONTROL
DATA
DC CONTROL
DATA
DC CONTROL
ECC-PARITY
DC CONTROL

FIG.3

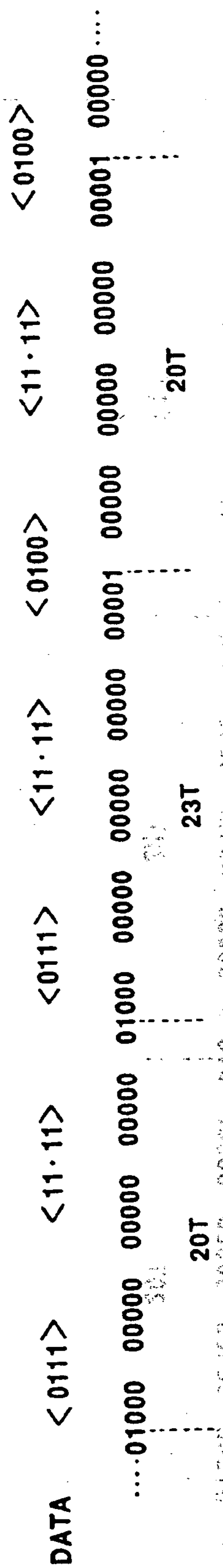
DATA
<0111>
<11·11>
<0111>
<11·11>
<0100>
<11·11>
<0100>
····01000 00000 00000 00000 01000 00000 00000 00000 00001 00000 00000 00000 00001 00000····
20T
23T
20T

FIG.4

```
DATA   <0111>         <11·11>        <0111>         <11·11>        <0101>         <11·11>        <0100>
   ····01000  00000  00000  00000  01000  00000  00000  00000  00010  00000  00000  00000  00001  00000····
             20T                           22T                           21T
```

FIG.5

NRZ DATA · · · 0 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 1 1 1 · · ·

NRZI DATA · · · 0 1 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1 0 0 · · ·

FIG.6

NRZ DATA

5T 23T 17T

00000 11111 11111 11111 11111 11100 00000 00000 00000 11 · · ·

NRZI DATA

10000 10000 00000 00000 00000 00010 00000 00000 00000 10 · · ·

FIG.7

NRZI DATA · · · 0 1 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1 0 0 · · ·

COUNT · · · · 0 1 2 3 4 5 6 0 1 2 3 4 5 6 7 8 0 1 2 · · ·

LATCH · · · · · · · · 6 6 6 6 6 6 6 6 6 6 8 8 · · ·

FIG.8

NRZI DATA

10000 00000 00000 00000 00010 00000 00000 00000 00001 · · · ·

23T 21T

FIG.9

NRZI DATA	10000 10000 00000	0 0 0 1 0 00000	0000 1 00000 10000 10 ··
COUNT	01234 01234 56789	2021220 1 23456	17181920 0 12345 01234 01 ··
LATCH	·········44444 44444	44422 22·····22	2222222220 20·····20 55555 44 ··

ta

tb

FIG.10

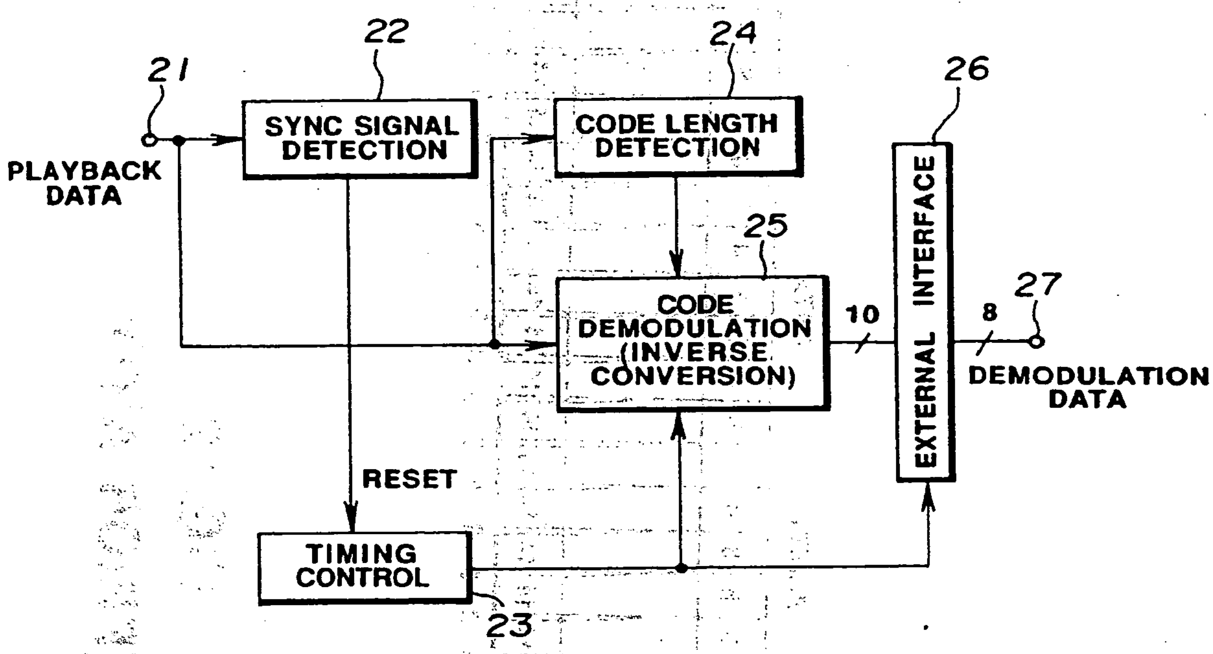
21
22
24
26
25
27
23
SYNC SIGNAL DETECTION
CODE LENGTH DETECTION
PLAYBACK DATA
CODE DEMODULATION (INVERSE CONVERSION)
10
8
EXTERNAL INTERFACE
DEMODULATION DATA
RESET
TIMING CONTROL

FIG.11

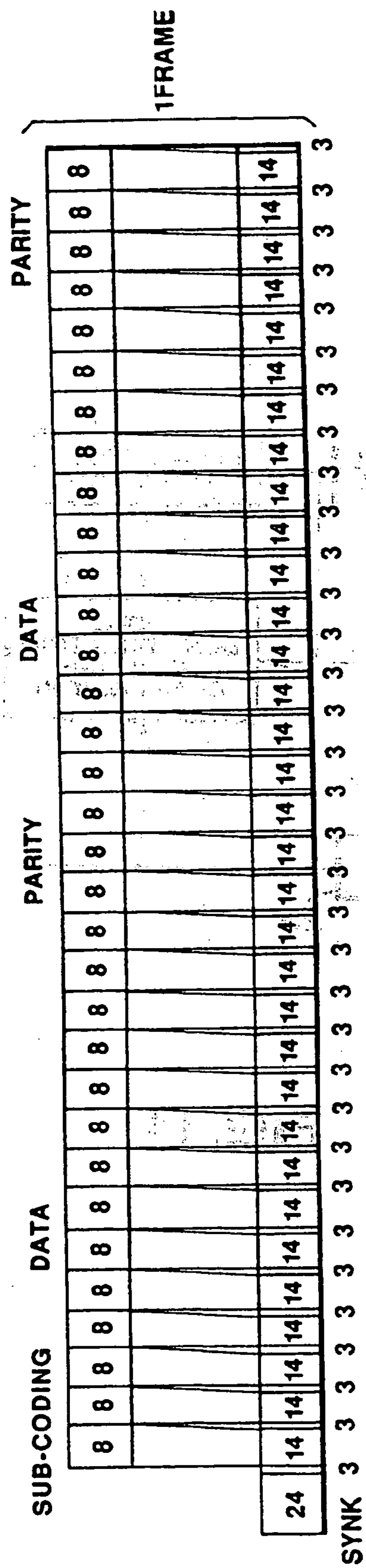

FIG.12
(PRIOR ART)

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Office européen des brevets

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(54) Synchronization signal detector, synchronization signal detecting method and demodulator.

(57) A synchronization detector includes a NRZI circuit (2) for extracting edge portions of RF signals detected as binary-valued signals to form a pulse train, a counter (6) for counting the number of channel clocks in the distance between transitions represented by the edge portions, a latch circuit (5) operated responsive to pulses from the NRZI circuit for holding a number of previously counted channel clocks immediately preceding a current count of channel clocks, and AND gates (7, 8, 9, 10, 11, 12) and an OR gate (13) for detecting synchronization signals when the combination of the channel clocks from the counter and the latch circuit is the combination of the maximum distance between transitions Tmax and Tmax-kT (k = 1 or 2) of a (d, k ; m, n ; r) modulation code. Synchronization signals may be detected promptly even if the frame structure is increased in size to enable restoration of synchronization to be expedited when frame structure synchronization is not in order. A demodulator utilizing the synchronization signal detector is also disclosed.

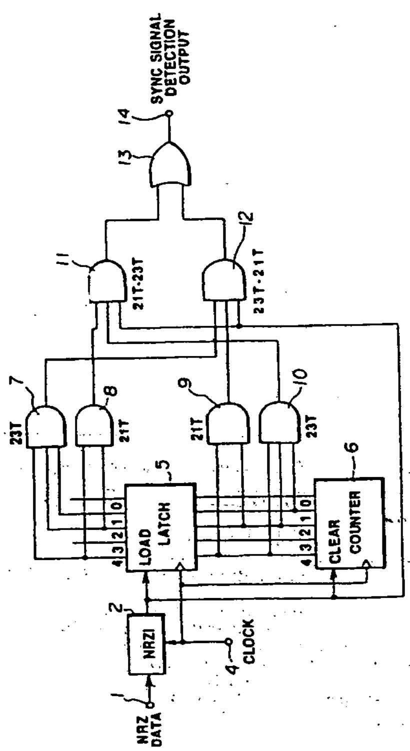

FIG.1

EP 0 577 402 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 30 5100

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X	PATENT ABSTRACTS OF JAPAN vol. 11, no. 70 (E-485) (2517) 3 March 1987 & JP-A-61 225 920 (TOSHIBA) 7 October 1986 * abstract *	1	G11B20/10 G11B27/10 G11B27/30
Y		2,7-9	
Y	EP-A-0 455 267 (SHARP) * column 3, line 9 - column 4, line 15 * * figures 1-3 *	2,7-9	
A	US-A-5 062 011 (HASE ET AL) * abstract; figures 1,2,5 *	2,9	
			TECHNICAL FIELDS SEARCHED (Int.Cl.5)
			G11B H03M H04L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	17 May 1994	Jonsson, P.O.

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